A Case for 3D Stacked Analog Circuits in High-Speed Sensing Systems

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Abstract—In order to build high performance real-time sensing systems every building block in the system should be built with a technology that allows that building block to achieve its best performance. Technologies like BJT and BICMOS are better suited for building basic analog blocks like input buffers and power amplifiers, while CMOS is the best choice for digital data processing. To build mixed-technology systems traditionally system-in-package (SiP) techniques are used. SiP integration uses bonding wires or flip chip instead of on-chip integration. In this paper we study the feasibility of using 3D stacking to integrate heterogeneous blocks built using different technologies within a real-time sensing system. Several of the previous studies on 3D stacking focused on integrating multiple digital blocks and using through-silicon-vias (TSVs) to transfer digital signals between the layers in a stack. In this paper we study the behavior of the analog signals traversing through TSVs and measure how well 3D stacking can enhance or limit the performance of analog and digital stacking. In order to quantify the power and performance characteristics, we modeled bonding wire, flip chip, and through-silicon-via (TSV) interfaces. Using these models we show that 3D stacking of analog and analog/digital components can double the bandwidth, increase sampling frequency by nearly two orders magnitude and and improve the signal integrity by 3 dB compared to bond wires.

Keywords— 3D stacking, bonding wire interface, analog-analog stacking

I. Introduction

The role of computers systems is continually being redefined as each usage model matures and a new usage model starts to dominate. One emerging domain of interest is high-performance real-time sensing systems that interface physical and digital worlds. In these systems a computing node reads and responds to very high bandwidth analog signals, such as radar data, from the physical world. These systems receive analog data and process the analog signals through components such as amplifiers, analog to digital data converters (ADC) and filters. These components play a critical role in sensing the analog signals in the physical world, cancel out unwanted signals, and amplify the signal so it will be accurately translated into its digital representation. The digital representation of the data is analyzed on a processor core. As the popularity of these systems grow, there is an increasing demand for higher resolution and high speed data converters, efficient sensors, and higher performance processing units.

CMOS technology scaling has benefitted the digital processing components of these cyber-physical systems. CMOS scaling has also benefitted low-mid resolution ADCs (widely used in communication systems), particularly when augmented with digital calibration techniques [1]. However, scaling has delivered non-uniform benefits to other analog components designs, such as high speed buffers used to capture incoming analog signals.

To justify our claim that CMOS scaling does not benefit all analog components, Table I shows how several important analog properties scale with technology. These results are based on ITRS projections [2] and some of our simulation data using PTM model [3]. Analysis of the analog characteristics of the transistors in sub-100nm technologies shows that, some of the critical device properties, such as available voltage headroom, transistor conductance, transistor intrinsic gain and 1/f noise actually worsen with scaling, which negatively impacts analog designs such as input buffers. However, ideal transistor speed (f_T) improves with scaling, which are exploited by some ADC designs, such as flash ADCs. Similarly, A_{vt} is the threshold voltage mismatch parameter, which has stayed relatively constant with process generation. Threshold voltage variation is proportional to A_{vt}, while it is inversely proportional to the square root of transistor width and length. With fixed value of A_{vt} and continuous decrease in device dimensions the threshold voltage variation is expected to increase with smaller device dimensions. In essence, transistors under different stress levels will have different degradation levels in smaller technologies. So, the mismatches between transistors will increase causing a limitation on the circuit lifetime functionality. While CMOS suffers from these analog scaling impediments, alternative technologies such as BJT do not suffer as much from mismatch [4].

To illustrate the point that different technologies are suited for building different analog building blocks, consider an input buffer that receives an analog signal as input. Ideally we want the input buffer to have the highest drive strength, which can be measured using g_m/I_d metric, where g_m is the transconductance and I_d is the DC current. Figure 1 shows the g_m/I_d metric for a single transistor built from four different CMOS generations and BJT. It is clear from the figure that the driving capability for the CMOS devices will get worse with scaling while the driving capability of BJT stays constant.

Thus, technology scaling makes CMOS not always the best choice for building many emerging real-time sensing systems. Technologies such as BJT and BICMOS are better suited for building analog blocks like input buffers and power amplifiers. It is therefore necessary to combine the most appropriate technology for each building block to build future real-time sensing systems. As such designers are increasingly relying on system-in-package (SiP) solutions where every component is manufactured using a process technology that is most appropriate for that component. These components are then integrated using bond-

TABLE I
TECHNOLOGY SCALING TRENDS

Tech Node	Vswing	Gds (mΩs)	Intinsic Gain (dB)	A_{vt} Match	Max Fre (GHz)
90nm	0.83	1.63e-04	20	6	170
65nm	0.73	2.00e-04	18	5	240
45nm	0.62	2.62e-04	15	5	320
32nm	0.53	3.47e-04	12	5	400

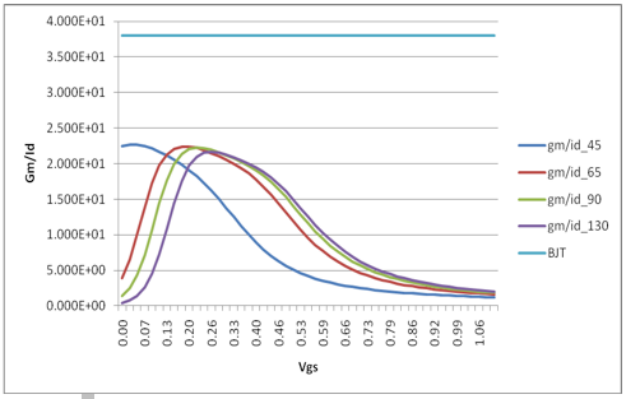

Fig. 1. Scaling impact on transistor efficiency

ing wires. However, SiPs suffer from significant wire parasitic as signals cross chip boundaries. Under these conditions, 3D stacking is a promising technology that allows us to integrate two or more dies vertically through high speed interconnects. In particular, 3D stacking can be used to integrate analog and digital components into a single die using through-silicon-vias (TSVs). 3D stacking has been proposed to stack processors and memory, in order to mitigate the wire scaling issues before [5], [6], [7]. The goal of this paper is to quantify the power and performance benefits of TSV-centric 3D integration of future analog-analog/digital interface systems.

The rest of the paper is organized as follows: In Section II we discuss the basic analog blocks used in the high speed sensing systems and analyze their required technology features. In Section III we discuss the lumped models for the TSV and the bonding wires that will be used to integrate these building blocks. In section IV we evaluate the integrated system in terms of area, power, signal integrity and supported bandwidth.

II. Design Methodology

Figure 2 shows the target system under study. The main analog blocks of the data acquisition systems are the input buffer and the analog to digital data converter. In high speed and high throughput systems, like radar and real time oscilloscopes, the input signal arriving at the analog front-end usually has a bandwidth in multi GHz. Handling such high speed signals requires high speed buffers and fast data converters. The data is then fed to a back-end digital system for further processing. We assume that there is sufficient digital processing capability and hence focus only on the analog front-end. The accuracy of the overall sensing system depends on the quality of the data provided by the analog front-end.

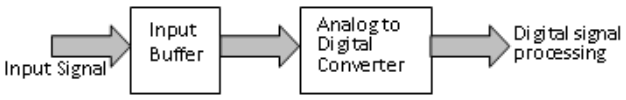

Fig. 2. Basic building blocks for data acquisition systems

A. Input Buffer

In order to achieve the goal of transferring the signal without affecting its linearity and amplitude, an input buffer is used in the front-end. Infinite input resistance, zero output resistance, perfect linearity, instant output response and supporting wide range of frequencies are important characteristics of an ideal input buffer. In order to achieve these goals a closed-loop operational amplifier or open-loop cascaded amplifiers are commonly used at the analog front-end.

$$gm(BJT) = q * I_c/kT \quad (1)$$

$$gm(FET) = Const * \sqrt{(I_d)} \quad (2)$$

To achieve near-ideal characteristics the input buffer can be implemented using Bipolar Junction Transistors (BJT). BJT provides higher gain than CMOS transistors. The reason for the higher gain is that BJTs transconductance is directly proportional to the DC current of the collector, while CMOS transconductance is proportional to the square root of the drain DC current[8]. Hence, for the same current, BJT transistors have much higher transconductance than MOS transistors, which translates into higher gain, speed and lower noise [2], [9]. BJT, on the other hand, has smaller input resistance and larger input current thereby demanding much higher power consumption. CMOS input buffers have an infinite input resistance and zero input current. Hence, CMOS technology is more appropriate to be used at the input stage of the input buffer. On the other hand the BJT characteristics of the transistor are more appropriate to be available at the output stage of the input buffer. Hence, integrating CMOS with BJT provides an ideal solution in terms of signal integrity and the range of supported frequencies. BICMOS process which is introduced by IBM can be used to integrate both BJT and CMOS transistors on the same chip to build the input buffer required in high speed systems, but it comes at a significantly higher cost. In [8] the authors studied different figure of merits required to build high speed system (noise, matching and gm) and concluded that BICMOS process is better, if manufacturing cost is not a primary concern.

B. ADC

The second component in our study is the ADC. It has been shown in [1] that high speed but moderate-to-low (7-bit) resolution ADCs can be built with CMOS in deep submicron tech-

nologies, when augmented with digital calibration support. In particular, a differential clock boot strapped sample and hold circuit built using 45nm technology has been shown to meet high speed demands while overcoming charge injection, clock feed through and the other non-idealities introduced by CMOS in deep submicron technology. The target specifications of the sample and hold circuit are listed in Table II . Note that ENOB is the Effective Number of Bits (also called ADC resolution). These parameters are minimum requirements for ADC to handle multi GHz data sensing systems [10].

TABLE II
SPECIFICATIONS FOR S/H CIRCUIT

Signal frequency	3GHz
Sampling frequency	10GHz
Sampling Capacitance	4pF
Technology	45nm
ENOB	7-bits
Tracking BW	$>$ 5Ghz

C. System Integration

The last step in the design is to integrate the input buffer with ADC. The data buffered in the input buffers is fed as input to high speed ADCs. In essence, the input buffer needs to be interfaced with ADC. System integration of two analog components with very different technology demands is an ideal place to use 3D stacking. For instance, input buffers can be built using a combination of BJT and CMOS technologies, while ADCs can exploit CMOS technology when augmented with digital calibration. In fact significant research effort is spent on designing ADCs with advanced process technology nodes.

We explore three options for system integration in this study. The first option is that the two blocks, input buffers and ADCs, are integrated using bonding wires. The second option is to use the flip chip and the silicon interposer to integrate multiple dies together; for simplicity we will refer to this design simply as flip chip through out this paper. The third option integrates the two blocks using TSV into a 3D stack. In order to accurately quantify the cost-benefit analysis of 3D integration versus off-chip bonding we modeled the wire parasitic as described in the next section.

III. Interface Modeling

A. Bonding Wire Model

The bonding wires are modeled as an inductance in series with a small resistance terminated with the equivalent capacitance of the sender and receiver pads. Figure 3 shows the lumped RLC model for the bonding wires. Table III shows the lumped model parameters for the bonding wire.

L_{bond}**:** As commonly assumed, we use bonding wire inductance to be 1nH/mm. Bonding wire lengths vary significantly depending on packaging and bonding technology. Hence, in our experiments we varied the values for the bonding wire lengths from .5mm to 2mm, and as a result the inductance ranges from .5nH to 2nH. As we will show later, the bonding wire inductance will be the dominant factor in controlling system performance

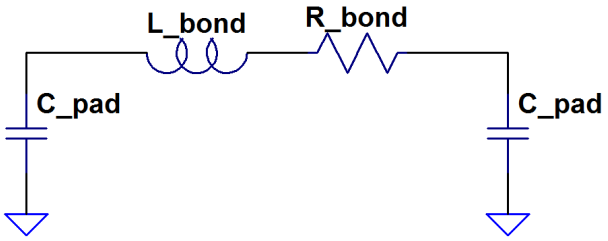

Fig. 3. Lumped RLC model of bonding wire

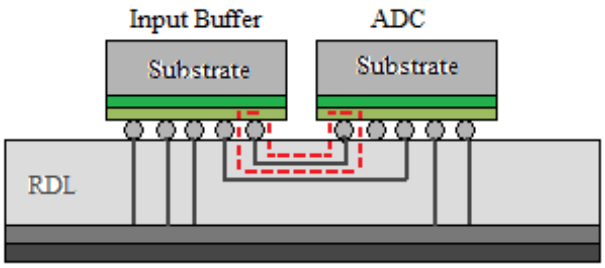

Fig. 4. The Structure of a flip chip Integration

R_{bond}**:** The value of the bonding wire resistance is small due to its large cross sectional area; in our simulations we used a 25um bonding wire that has a 10mΩ/mm resistance. Changing the bonding wire length in our experiments changes the bonding wire resistance by few milli-ohms.

C_{pad}**:** C_{pad} is used to model the capacitance of the sender and the receiver pads

TABLE III
BONDING WIRE RLC PARAMETERS

diameter	25um
length	1mm
L_{bond}	1nH
R_{bond}	10mΩ
C_{pad}	100fF

B. Flip Chip

In order to reduce the interface parasitics, flip chip technology can be used. In flip chip integration the dies are flipped and attached to the silicon interposer to connect the integrated dies together. In order to model flip chip integration a lumped RLC model is developed for the highlighted area (in dotted line) in Figure 4.

The interconnection includes the micro-bumps and the redistribution layer(RDL). The micro-bump lumped RLC model is similar to the one developed to the bonding wire, except that the length of wire is shorter in the micro-bump model. The RLC values of the micro-bumps are listed in Table IV. In addition, the low latency RDL is modeled using a lumped RC model using the values obtained from [11].

C. TSV Wire Model

The critical element in the 3D-ICs is the TSV model that replaces the bonding wires used in connecting the dies. An initial

TABLE IV
MICRO-BUMP PHYSICAL DIMENSIONS AND RLC VALUES

diameter	25-50um
length	.1mm
L_{Flip}	80pH
R_{Flip}	30mΩ
C_{pad}	100fF

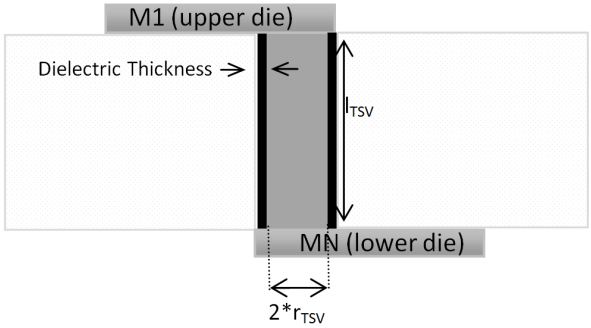

Fig. 5. TSV Structure Modeled

model for TSV inductance, resistance and capacitance was provided in [12]. This model has been shown to match real implementations for diameters less than 10um. But this model does not take into account skin effects on TSV, which cause additional parasitic overhead, when operating at high frequency. Hence, we modified the base model in [12] to take skin effect of the TSV into considerations. Figure 5 shows the cross-section view of the TSV and its important dimensions that will be used in our equations to calculate different elements of the lumped model.

L_{TSV}**:** The inductance value of TSV depends on the geometry of the TSV (radius and length) in addition of the permeability of the surrounding medium. we used the inductance equation in [13] to calculate the self-inductance in our experiments.

R_{TSV} The resistance for the TSV is calculated using the traditional equation for the cylindrical resistance.

$$R_{TSV} = l_{TSV}/\sigma * \pi * r_{TSV}^2 \tag{3}$$

Where σ is the filling material conductivity, l_{TSV} is the TSV length, and r_{TSV} is the radius. From the equation it is clear that the value of the resistance depends on the radius and the length of the TSV. For high frequency systems, similar to the domain we are targeting, the skin effect should be taken into consideration. In short, skin effect reduces the effective radius of the TSV since the charge starts to flow only on the surface of the TSV at high frequency. As such the effective resistance of the TSV will increase. For example, the skin depth is 5um at 738 MHz, while the skin depth reduces to 2um at 4.71 GHz [14]. We modeled two different TSV diameters: 5um and 2um. Given that skin depth effect does not impact 2um TSV we only consider skin depth effect when modeling the 5um TSV.

The skin effect is modeled by connecting a series inductance and resistance in parallel with the R_{TSV} as shown in Figure 6. The value of R_{skin} and L_{skin} are calculated using the equation in [15]. In addition, the substrate resistance depends on the number of body contacts surrounding the TSV. Its value may range from 1.5kΩ , when no body contacts surrounding the TSV, to

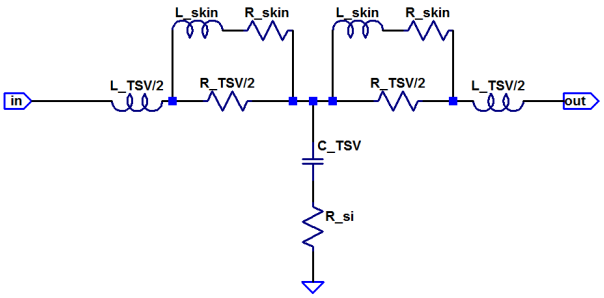

Fig. 6. Lumped RLC model of TSV

50Ω when the TSV it is surrounded by 4 body contacts [16]. Based on ITRS 2010 predictions [2], we used 50u TSV length in our experiments. With the improvements in the 3D integration process we expect to see a thinner wafers and as a result a shorter TSVs in future.

C_{TSV}**:** We assume that TSVs are far separated from each other on a die and hence do not have coupling capacitance. C_{TSV} has two components. The first component is the insulator capacitance, which is formed between the TSV metal and the silicon substrate. The second component is depletion capacitance, which depends on the width of the depletion around the TSV. The width of the depletion region depends on the thickness of the oxide surrounding the TSV and the biasing voltage of the TSV. Thus, the capacitance of TSV can be represented as a parallel combination of the insulator capacitance and the depletion capacitance.

$$C_{TSV} = (C_{INS} * C_{DEP})/(C_{INS} + C_{DEP}) \tag{4}$$

Where C_{INS} is the insulator capacitance and C_{DEP} is the depletion capacitance. Due to the dependence of the C_{DEP} on the biasing voltage across the TSV, C_{DEP} can be formed in the accumulation, depletion or the inversion regions. Thus the dependency on biasing voltage leads to non-linearity, which may affect the performance and the characteristics of the signal that passes through the TSV. In order to account for this dependency, in our simulations we vary the TSV capacitance between C_{INS} and $C_{INS}/2$ as suggested in [12].

To summarize, Figure 6 shows the entire lumped model used to model TSV in our simulations. The calculated values for R_{TSV}, L_{TSV} and C_{TSV} are listed in the table V for TSV diameter of 5um and length of 50u. These values give us an indication about the TSV parasitic compared with values used for the bonding wire and flip chip.

TABLE V
TSV MODEL PARAMETERS

di-electric thickness	100nm
diameter	5um
length	50um
L_{TSV}	34pH
R_{TSV}	44mΩ
C_{TSV}	200fF

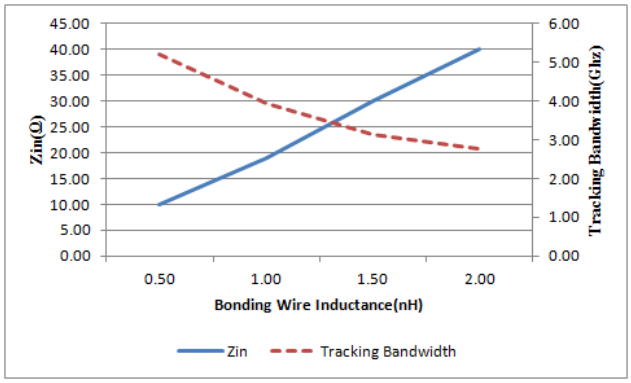

Fig. 7. Bonding wire input impedance and tracking bandwidth

IV. Simulation Results

In our simulation experiments we will compare the three configurations under study, namely bonding wires, flip chip and TSVs to combine the CMOS input buffer with ADC. We will compare the results in terms of supported bandwidth, power consumption, area overhead and signal integrity.

A. Bandwidth

Bandwidth plays a main role in deciding the maximum signal frequency that can pass through the interface without being attenuated. The bandwidth depends mainly on the input impedance seen at the output of the buffer for the frequency of interest. Figure 7 shows the relationship between input impedance and attainable bandwidth for the bonding wire model at 3 GHz. The X-axis refers to the bonding wire inductance value (which is essentially the length of the wire), the primary Y-axis refers to the input impedance and the secondary Y-axis refers to the tracking bandwidth. As shown, increasing the value of the inductance by increasing the wire length, plays a main role in controlling the bandwidth characteristics of the integrated system. We also measured the input impedance and tracking bandwidth of flip chip using parameters listed in Table IV and TSV designs using the parameters listed in Table V. Our results show that the impedance of the TSV at 3Ghz equal 1.25Ω which is at least eight times lower than than the impedance of the shortest bonding wires, and is three times lower than that of the flip chip design.

In order to measure the interface impedance effects on the tracking bandwidth we used an idealized switch that is interfaced with the input buffer. The interface uses a bonding wire, flip chip or a TSV in our experiments. The idealized switch has 1Ω ON resistance terminated by 4pF load capacitance. The exact load capacitance depends on the sampling capacitance of ADC, which may vary from one design to another. Hence, we selected 4pF just as one design choice.

Figure 7 shows the tracking bandwidth on the secondary Y-axis for different inductance values of bonding wires (different bonding wire lengths). The results show that the tracking bandwidth degrades significantly with increasing bonding wire length due to the increase in the input impedance, marked as Z_{in} in Figure 7 . This degradation may cause a major limitation in building systems that support high frequency signals. Results from flip-chip design show 7.8 GHz tracking bandwidth, which is only better than the best bandwidth obtained through bonding wires. On the other hand the 5um TSV achieved 11 GHz tracking bandwidth in our simulations, which is at least twice as much bandwidth as the best bonding wire design.

It is also interesting to note in our simulations we noticed that even for the same tracking bandwidth, the system built using bonding wires shows an overshoot in the frequency response that may affect the linearity of the system. On the other hand, there is no overshoot in the frequency response of the system using TSVs due to the small inductance values of the TSVs.

The value of the RC also determines the minimum tracking time for the ADC to achieve n-bit accuracy. For example, 6.9 RC time constants are required to achieve 0.1% accuracy required by the 10-bit ADC. As a result, having a high RC time constant may pose limitations on the maximum sampling frequencies. So, the RC of the circuit can control the max input frequency that the circuit can support. For example for a 10-bit accuracy system, Table VI shows the maximum input sampling frequency (F_s) supported by the system integrated using different configurations of the bonding wire, flip chip and TSVs.

TABLE VI
MAXIMUM SAMPLING FREQUENCY: 10-BIT S/H WITH RC=6.9

Interface	R(Ω)	F_s
$Bond_{L=2nH}$	40	5.77E+08
$Bond_{L=1.5nH}$	30	7.69E+08
$Bond_{L=1nH}$	19	1.21E+09
$Bond_{L=.5nH}$	10	2.31E+09
$FlipChip$	4.5	5.13E+09
$TSV_{D=5um}$	1.25	18.5E+10

B. Power

The power consumed by ADC and the input buffer is about three orders of magnitude higher than the interface power. Hence, we assume that a system that used either bonding wire,flip chip and TSV may consume the same power. However, a TSV based system provides much higher bandwidth as described above. Thus a designer may tradeoff higher bandwidth of TSV design with lower system power. For example, to obtain 4 GHz tracking bandwidth, the system integrated using the TSV will consume 10X less power when compared with the system built using a 1nH bonding wire. This difference comes from the dominance of the bonding wire impedance that neglects the saving in impedance obtained from reducing the buffer and the sample and hold resistances. On the other hand, due to its smaller parasitics and AC resistance when compared to bond wires, the flip chip interface consumes less power than bonding wire, but it still consumes 33% more power when compared to a TSV design.

C. Signal Integrity

Signal integrity is another metric that can be used to evaluate a system interfaced using either bonding wires, flip chip or TSV. The signal integrity is measured using two well known metrics, Spurious-Free Dynamic Range (SFDR) and signal to noise and distortion ratio (SNDR). The transient noise is taken

into consideration during simulations to get accurate measurement. In order to evaluate these effects the ideal switch in the previous configuration is replaced by the real sample and hold circuit (S/H) built using 45nm technology. Table VII lists the measured SNR and SFDR for different configurations. First row in the table shows the calculated values when no interface used. When bonding wire is used, the results show that the value of the SNDR is less and varies by 4 dB for different values of the bonding wire inductance. This variation will affect the Effective Number of Bits (ENOB) metric when bonding wire is used for integration. If SNDR reduces by about 6 dB, ENOB drops by 1 bit. In addition, flip chip shows a 2.5dB degradation in the SNDR. On the other hand, when using TSV integration the results obtained are similar to the no-interface case. In addition, the variation in the SNDR for the 5um and 2um TSVs is within 0.1dB. As mentioned earlier TSV capacitance can vary with bias voltage. Hence, we varied the TSV capacitance by a factor of 2 [12]. The results show a variation of 0.1 dB in the case of 5um TSV.

TABLE VII
SIGNAL INTEGRITY MEASUREMENTS

Interface	SFDR	SNDR
Ideal	44	42.1
$Bond_{L=2nH}$	40	35.9
$Bond_{L=1nH}$	42	39.2
$Bond_{L=.5nH}$	43	39.6
$FlipChip$	42	39.5
$TSV_{D=5um,C=C_{INS}}$	44	41
$TSV_{D=5um,C=C_{INS}/2}$	43	41.1
$TSV_{D=2um}$	43	41

V. Conclusions

In this paper we first make a case that CMOS scaling has non-uniform impact on different analog components used in high-speed real-time sensing systems. While some analog components benefit from CMOS other components suffer from the side effects of CMOS scaling. Some analog components benefit from using technologies such as BJT. Hence, we argue that heterogeneous technology integration provides the best opportunity to use appropriate technology for each basic building block. We then evaluated 3D stacking as an attractive alternative to System-in-Package (SiP) solutions that are traditionally used to integrate heterogeneous process technologies. We present a detailed analysis and experiments to compare designs integrated using the bonding wires against those integrated using TSVs in terms of bandwidth, power, and signal integrity. In our experiments we targeted a high-speed and high-throughput systems such as those used in the radar systems. The experiments show that the high impedance of the bonding wires and flip chip interface limits their usability in such systems. On the other hand, TSV integration shows promising benefits due to its low parasitics. As a result, TSV can be a suitable interface to be used to meet the increasing demand for high-speed real-time sensing systems.

VI. Acknowledgements

This material is based upon work supported by the National Science Foundation under Grants No. CNS-0834798 and CCF-0954211.

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